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In the Office Action, the Examiner rejected claims 1-3, 5-15, 17-24 and 26-30 under 35 U.S.C. 102(b) as being anticipated by *Williams* (U.S. Pat. No. 5,898,895); and rejected claims 4, 16 and 25 under 35 U.S.C. 103(a) as being unpatentable over *Williams* in view of *Malek* (U.S. Pat. No. 5,086,467). Applicants traverse the rejections for the reasons set forth below. Reconsideration is respectfully requested based on the remarks below.

Claims 13, 16-20, and 21 have been amended to further clarify the subject matter regarded as the invention. Support for the amendments can be found in original claims 15-20 and elsewhere. Claim 15 has been canceled without prejudice. Accordingly, claims 1-14 and 16-30 are now pending in this application.

PATENTABILITY OF CLAIMS 1-14 AND 16-30

Original independent claim 1 is directed to a method for testing arbitration logic or bus-mastering logic associated with a digital logic device. The method includes among other things the limitations of “determining a pseudo-random delay prior to responding to the request” and “pseudo-randomly delaying a response to the request.”

Original independent claim 28 is directed to an apparatus for testing arbitration logic associated with a programmable chip system. The apparatus includes among other things the limitations of “means for determining a pseudo-random delay prior to responding to the request” and “means for pseudo-randomly delaying a response to the request.”

Amended independent claim 13 is directed to a secondary component. The secondary component includes among other things the limitation of “a delay mechanism configured to determine values operable to delay responses to requests received through the interconnection module, wherein the values are pseudo-randomly generated values.”

Amended independent claim 21 is directed to a programmable chip. The programmable chip includes among other things the limitation of “wherein the plurality of secondary components are configured to determine delay values for adjusting response times to requests received through arbitration logic, wherein the values are pseudo-randomly generated values.”

In the Office Action, the Examiner cited *Williams* as disclosing a “pseudo-random delay.” (See page 2, last paragraph to page 3, paragraph 2) Specifically, the Examiner stated that “[a] pulse generator 170 generates plurality of delay pulses corresponding to a “pseudo-random delay”, shown as DELAYS 1-4, since the delay requirement can be randomly selected depending on the clock speed.” It is respectfully submitted, however, that the DELAYS 1-4 do

not correspond to the pseudo-random delay limitations as recited in independent claims 1, 13, 21, and 28. For example, *Williams* does not teach or suggest that DELAYS 1-4 are “pseudo-randomly generated values”.

Williams discloses that the pulse generator 170 receives a read request signal 134 and “generates a plurality of signal pulses in response thereto.” *Williams* also discloses that “each of the pulses occurs at a different *predetermined time* from the occurrence of the read request signal” and that “[o]ne of the pulses is selected to be the read acknowledge signal, which allows the read request buffer queue to output another read request signal.” (See Abstract; column 2, lines 40-47) Since each of the pulses corresponding to DELAYS 1-4 occurs at a “*predetermined time*,” DELAYS 1-4 are not pseudo-randomly generated values. In fact, as shown in Fig. 8, pulses Phase-A, Phase-B, Phase-C, and Phase-D corresponding to DELAYS 1-4 respectively are predetermined delays based on fixed clock pulses (e.g., t=1, t=2, t=3, t=4, t=5). (See column 8, lines 44-59)

Although the Examiner asserts that “the delay requirement can be randomly selected depending on the clock speed,” nowhere in *Williams* remotely suggests this assertion. *Williams* merely states that “[t]he read acknowledge signal is generated at a *predetermined time* from the occurrence of the data request signal, and this *predetermined time* can be modified to correspond to the amount of data transmission delay desired.” (See column 2, lines 63-66) This only suggests that the predetermined time can be modified such that the amount of data transmission delay is controlled. (E.g., see column 8, line 60 to column 9, line 13) In fact, *Williams* states that “[t]he read acknowledge signal on line 136 can be delayed in time to most closely match the speed difference between the clock domain 110 and the clock domain 114.” (See column 6, lines 19-22) As such, an orderly controlled selection of a fixed/predetermined time delay (as opposed to a random time delay) for the read acknowledge signal is needed for matching the speed difference between the clock domain 110 and the clock domain 114.

Even though *Malek* discloses a linear feedback shift register (LFSR) for generating a pseudo-random sequence, there is no motivation to combine the teachings of *Malek* with the teachings of *Williams*. This is because, as described above, *Williams* teaches away from using pseudo-random generated values for producing a delayed read acknowledge signal. That is, the system for providing speed-regulated data transmission between two synchronous systems in different clock domains as disclosed in *Williams* will not work with the LFSR as disclosed in *Malek* since a pseudo-random sequence will produce a delayed read acknowledge signal that is unlikely to match the speed difference between the clock domains. In view of the above, it is respectfully submitted that independent claims 1, 13, 21, and 28 are patentable over the cited art.

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The Examiner's rejections of the dependent claims are respectfully traversed. Claims 2-12, 14, 16-20, 22-27, 29 and 30 each depend either directly or indirectly from independent claims 1, 13, 21, or 28 and, therefore, are respectfully submitted to be patentable over cited art for at least the reasons set forth above with respect to claims 1, 13, 21, or 28. Further, the dependent claims require additional elements that when considered in context of the claimed inventions further patentably distinguish the invention from the cited art.

SUMMARY

It is respectfully submitted that all pending claims are allowable and that this case is now in condition for allowance. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

If any fees are due in connection with the filing of this Amendment, the Commissioner is authorized to deduct such fees from the undersigned's Deposit Account No. 500388 (Order No. ALTRP112).

Respectfully submitted,
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